IN THE CLAIMS

1-9. (Cancelled)

10. (Original) A method of manufacturing a semiconductor device, comprising:

preparing a semiconductor device having a cell array region and a peripheral circuit region;

sequentially forming a gate insulating layer and a gate conductive layer on the semiconductor substrate;

forming a word line capping layer and a gate capping layer on the gate conductive layer;

patterning the word line capping layer, the gate capping layer, and the gate conductive layer to form a plurality of word line patterns in the cell array region and at least one gate pattern in the peripheral circuit region, the word line pattern including a word line and a word line capping layer pattern, the gate pattern including a gate electrode and a gate capping layer pattern;

forming gate spacers on side walls of the word line pattern and the gate pattern;

sequentially forming a pad interlayer insulating layer and a bit line interlayer insulating layer over a surface of the semiconductor substrate having the gate spacers; and

patterning the bit line interlayer insulating layer, the pad interlayer insulating layer, and the gate capping layer pattern to form a cell contact hole penetrating a region between the word line patterns and a peripheral circuit contact hole exposing the gate electrode.

11. (Original) The method of claim 10, wherein forming the word line capping layer and the gate capping layer on the gate conductive layer comprises:

etching the word line capping layer in the peripheral circuit region to expose the gate conductive layer;

forming the gate capping layer with an etching selectivity ratio different from the word line capping layer over a surface of the semiconductor substrate; and

planarizing the gate capping layer to expose the word line capping layer in the cell array region while retaining the gate capping layer in the peripheral circuit region.

12. (Original) The method of claim 10, wherein forming the word line capping layer and the gate capping layer on the gate conductive layer comprises:

etching the gate capping layer in the cell array region to expose the gate conductive layer;

forming the word line capping layer with an etching selectivity ratio different from the gate capping layer over a surface of the semiconductor substrate; and

planarizing the word line capping layer to expose the gate capping layer in the peripheral circuit region while retaining the word line capping layer in the cell array region.

13. (Original) The method of claim 10, wherein patterning the word line capping layer, the gate capping layer, and the gate conductive layer comprises:

simultaneously patterning the word line capping layer in the cell array region and the gate capping layer in the peripheral circuit region to form the word line capping layer pattern and the gate capping layer pattern, respectively; and

etching the gate conductive layer by using the word line capping layer pattern and the gate capping layer pattern as a mask.

14. (Original) The method of claim 10, wherein patterning the word line capping layer, the gate capping layer, and the gate conductive layer comprises:

patterning the word line capping layer and the gate conductive layer in the cell array region to form the word line pattern; and

patterning the gate capping layer and the gate conductive layer in the peripheral circuit region to form the gate pattern.

15. (Original) The method of claim 10, wherein patterning the word line capping layer, the gate capping layer, and the gate conductive layer comprises:

in the peripheral circuit region, patterning the gate capping layer and the gate conductive layer to form the gate pattern; and

in the cell array region, patterning the word line capping layer and the gate conductive layer to form the word line pattern.

16. (Original) The method of claim 10, wherein forming the cell contact hole comprises forming the cell contact hole using a self-align method.

17. (Original) The method of claim 11, wherein etching the word line capping layer comprises using one chosen from the group consisting of a dry-etching process, a chemical mechanical polishing process, and a wet-etching process.

18. (Original) The method of claim 10, wherein forming the word line capping layer and the gate capping layer on the gate conductive layer comprises:

etching the word line capping layer in the peripheral circuit region to expose the gate conductive layer;

forming the gate capping layer with an etching selectivity ratio different from the word line capping layer over a surface of the semiconductor substrate;

forming a photoresist over the gate capping layer; and

etching back the photoresist and the gate capping layer in the cell array region to expose the word line capping layer.

19. (Original) The method of claim 12, wherein etching the gate capping layer comprises using one chosen from the group consisting of a dry-etching process, a chemical mechanical polishing process, and a wet-etching process.

20. (Original) The method of claim 10, wherein forming the word line capping layer and the gate capping layer on the gate conductive layer comprises:

etching the gate capping layer in the cell array region to expose the gate conductive layer;

forming the word line capping layer with an etching selectivity ratio different from the gate capping layer over a surface of the semiconductor substrate;

forming a photoresist over the word line capping layer; and

etching back the photoresist and the word line capping layer in the peripheral circuit region to expose the gate capping layer.

21. (New) A method comprising:

forming a gate insulating layer on a cell array region and a peripheral circuit region of a substrate;

forming a gate conductive layer on the gate insulating layer;

forming a word line capping layer on the gate conductive layer;

etching the word line capping layer to expose the gate conductive layer in the peripheral circuit region;

forming a gate capping layer on the word line capping layer in the cell array region and on the gate conductive layer in the peripheral circuit region;

planarizing the gate capping layer in the cell array region to expose the word line capping layer;

patterning the word line capping layer, the gate conductive layer, and the gate insulating layer in the cell array region to form word line patterns, the word line patterns having sidewalls;

patterning the gate capping layer, the gate conductive layer, and the gate insulating layer in the peripheral circuit region to form at least one gate pattern, the at least one gate pattern having sidewalls;

forming gate spacers on the sidewalls of the word line patterns and the at least one gate pattern;

forming a pad interlayer insulating layer that covers the word line patterns and the at least one gate pattern;

forming a bit line interlayer insulating layer on the pad insulating layer;

patterning the bit line interlayer insulating layer and the pad insulating layer to form a cell contact hole that exposes a portion of the substrate between the word line patterns; and

patterning the bit line interlayer insulating layer, the pad insulating layer, and the gate capping layer to form a peripheral circuit contact hole that exposes the gate conductive layer in the at least one gate pattern.